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for

**Area Efficient Waveform Evaluation and DC Offset Cancellation Circuits**

by

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## Field

**[0001]** Embodiments of the present invention relate to analog circuits, and more particularly, to analog circuits for providing waveform parameters.

## Background

**[0002]** Mixed signal circuits often evaluate several waveform parameters, such as, for example, the maximum, minimum, or average values, or the root-mean-square value. These waveform parameters are often evaluated in the analog domain because they are needed prior to A/D (analog-to-digital) conversion.

**[0003]** Typically, passive networks in combination with diodes (or diode-configured transistors) have been used to evaluate waveform parameters. For example, a typical averaging circuit is shown in Fig. 1, comprising resistor **102** and capacitor **104**. A peak detector circuit is shown in Fig. 2, comprising diode **202** and capacitor **204**. A nMOSFET (n-Metal-Oxide-Semiconductor-Field-Effect-Transistor) averaging detector is shown in Fig. 3, comprising nMOSFET **302** and parasitic capacitor **304**. The gate of nMOSFET **302** is biased to a bias voltage $V_{bias}$. In Fig. 3, the output network is indicated explicitly by Output Network block **306**, but it is implicit in the other figures.

**[0004]** Another common task in analog signal processing is the extraction of a waveform's DC (Direct Current) offset. DC offset extraction is often required for A/D conversion. Prior art DC offset extraction circuits may use passive networks. For example, the circuit of Fig. 1 may be utilized to provide a DC offset. An example of a typical prior art DC offset correction circuit utilizing an active device is shown in Fig. 4, where nMOSFET **402** is biased to a bias voltage $V_{bias}$. nMOSFET **402** and capacitor **404** provide an averaging circuit to provide a DC offset. DC Offset Correction block **406** provides the DC offset to Input Stage **410**, where it is subtracted from the input signal after passing through Input Stage **408**.

**[0005]** Prior art circuits such as Figs. 1 and 2 require components such as resistors or diodes, and may not be compatible with some low voltage CMOS (Complementary-Metal-Oxide-Semiconductor) process technology. Prior art circuits such as Figs. 3 and 4 require a bias voltage to bias nMOSFETs, adding to circuit complexity, and relatively large capacitances and low bias voltages may be needed to reject ripples below 1 KHz. It is advantageous to provide analog parameter evaluation circuits that take advantage of

sub-micron (e.g., less than 0.13 microns) CMOS process technology without requiring diodes and resistors, and without the need for large capacitances and a separate bias voltage.

## Brief Description of the Drawings

**[0006]** Fig. 1 is a prior art averaging circuit comprising a resistor and capacitor.

**[0007]** Fig. 2 is a prior art averaging circuit comprising a diode and a capacitor.

**[0008]** Fig. 3 is a prior art averaging circuit comprising a biased field-effect-transistor.

**[0009]** Fig. 4 is a prior art DC offset correction circuit comprising a biased field-effect-transistor.

**[0010]** Fig. 5 is an embodiment of the present invention for providing an output voltage indicative of a local time-average maximum of an input signal.

**[0011]** Fig. 6 is another embodiment of the present invention for providing an output voltage indicative of a local time-average minimum of an input signal.

**[0012]** Fig. 7 is another embodiment of the present invention for providing a voltage indicative of a local time-average of an input voltage for DC offset correction.

## Description of Embodiments

**[0013]** An embodiment of the present invention is shown in Fig. 5, comprising nMOSFET **502** and parasitic capacitor **504**, where the output network is indicated by Output Network block **506**. The gate of nMOSFET **502** is connected to terminal **508** of nMOSFET **502**. Terminal **508** may also be considered an input port to the circuit, or it may be considered connected to an input port. (Terminal **508** may also be referred to as input port **508**.) nMOSFET **502** is connected in a diode configuration. Output Network **506** may be capacitive in nature, or it may comprise repeated copies of MOSFETs and capacitor combinations. Output Network **506** may also include feedback connections to input port **508**.

**[0014]** The embodiment of Fig. 5 provides a maximum (or peak detection) function. More particularly, as described below, the embodiment of Fig. 5 provides a local time-average maximum (or local time-average peak detection) function, in the sense that it tracks a time varying maximum or peak of an input signal.

**[0015]** Consider first an initial state in which output port **510** is assumed to be at ground (substrate) potential and Output Network **506** is capacitive in nature. At input port

**508** let there be provided an input signal comprising the sum of an AC (Alternating Current) voltage component and a DC (offset) voltage component. For now, assume that the input signal is a stationary signal. Let the amplitude of the AC component be denoted as $V_{ac}$ and the DC voltage be denoted as $V_{dc}$. (The DC offset voltage may be viewed as an average voltage, or in the case of quasi-stationary signals, a local time-average voltage.) Then MOSFET **502** turns ON in response to the input signal, where terminal **508** acts as a drain and terminal **512** acts as a source to nMOSFET **502**. Output port **510** (and terminal **512** since port **510** and terminal **512** have the same potential) will charge up to $V_{dc} + V_{ac} - V_{th}$ , where $V_{th}$ is the threshold voltage of nMOSFET **502**.

**[0016]** Once output port **510** is charged to $V_{dc} + V_{ac} - V_{th}$ , then nMOSFET **502** is in its sub-threshold region. Suppose the input voltage were now to decrease (e.g., it is non-stationary). Viewing terminal **512** as the drain and terminal **508** as the source to nMOSFET **502**, it is seen that the gate-to-source voltage is zero. In that case, nMOSFET **502** is not turned ON. However, there is leakage (or sub-threshold) current that flows through nMOSFET **502**.

**[0017]** Note that once the voltage at terminal **512** reaches $V_{dc} + V_{ac} - V_{th}$, it will continue to increase with sub-threshold currents whenever the input voltage is higher than the output voltage. That is, it will charge up with sub-threshold currents defined by a gate-to-source voltage $V_{gs}$ where $0 < V_{gs} < V_{th}$. Then, whenever the input voltage is lower than the output voltage, the output terminal will be discharged by sub-threshold currents defined by a gate-to-source voltage of zero. Thus, the output voltage will converge to a local time-average maximum of the input signal, which will be the condition for which charging and discharging will occur with sub-threshold currents defined by gate-to-source voltages equal to zero. (For some communication applications, where $V_{ac}$ may be on the order of a few mV, this local time-average maximum value may be used as an approximate measure of the DC offset voltage.)

**[0018]** Variations in the input signal at input port **508** are tracked as fast as the leakage currents will allow. The embodiment of Fig. 5 takes advantage of sub-micron CMOS process technology, where the sub-threshold current may be in excess of 1 micro ampere per micron of device width. Such sub-threshold current may allow for tracking

input signal voltages at millisecond rates. The tracking rate may be controlled to be slower by adjusting the device length at minimum width.

**[0019]** With leakage current flowing through nMOSFET **502**, the effective resistance of nMOSFET **502** is higher than when nMOSFET **502** is ON, and the effective RC time constant for the combination of nMOSFET **502** and parasitic capacitor **504** may be made sufficiently large without requiring large capacitance. Input port **508** and output port **510** will switch between source and drain functionality, depending upon the relative polarities of input and output ports **508** and **510**, allowing the circuit of Fig. 5 to track a non-stationary (time varying) input signal via leakage currents through nMOSFET **502**.

**[0020]** Note that $V_{dc} + V_{ac}$ is the peak of a stationary input signal, so that the voltage $V_{dc} + V_{ac} - V_{th}$ is indicative of the maximum or peak. As described above, the circuit of Fig. 5 tracks non-stationary signals, in which case $V_{dc} + V_{ac}$ may be considered a local time-average maximum, so that the circuit of Fig. 5 provides a voltage indicate of a local time-average maximum of the input signal.

**[0021]** Another embodiment is shown in Fig. 6, where sub-threshold currents discharge node **604** if the gate-to-source voltage $V_{gs}$ of nMOSFET **602** is greater than zero, $V_{gs} > 0$, and charge node **604** if $V_{gs} = 0$, thus providing a local time-average minimum voltage detection function as now described.

**[0022]** In Fig. 6, the gate of nMOSFET **602** is connected to terminal **604**, which serves as output port **606**. Terminal **608** of nMOSFET **602** serves as an input port to the circuit. Consider the same initial state as considered for the circuit of Fig. 5, where output port **606** is assumed to be at ground (substrate) potential and Output Network **610** is capacitive in nature. At input port **608** let there be provided an input signal comprising an AC signal component with amplitude $V_{ac}$ and a DC offset (average) voltage $V_{dc}$. Then, terminal **608** may be considered the drain and terminal **604** may be considered the source. In that case, the gate-to-source voltage is zero and nMOSFET **602** is in its sub-threshold condition so that leakage current flows, and output node **606** charges. If the input voltage were to rapidly decrease more than $V_{th}$ below the gate voltage, then nMOSFET **602** will turn ON and conduct current to discharge terminal **604**. In this way, output node **606** will track the local time-average minimum of the input voltage to input port **608**.

**[0023]** Another embodiment is shown in Fig. 7, where charging and discharging sub-threshold currents balance each other to provide a local time-average voltage detection function (DC offset detection), which is now described.

**[0024]** Fig. 7 comprises a pair of sub-threshold active elements, nMOSFET **702** and nMOSFET **704**, for providing local time averaging. The gate of nMOSFET **704** is connected to one of its terminals, **706**, which is also connected to terminal **708** of nMOSFET **702**. The gate of nMOSFET **702** is connected to terminal **710** of nMOSFET **704** and to one of its terminals, **716**. Terminal **710** of nMOSFET **704** and terminal **716** of nMOSFET **702** are also connected to input port **714**. Capacitor **712** is connected to terminal **708**. The DC offset voltage is taken as the capacitor voltage, and is provided by DC Offset Correction **720** to Input Stage **718** where it is cancelled or subtracted from the input signal provided to input port **714**.

**[0025]** Assume that terminal **708** is initially at ground potential, and applied to input port **714** is an input signal comprising an AC voltage component with amplitude $V_{ac}$ and a DC offset (average) component with voltage $V_{dc}$. Then nMOSFET **702** turns ON and charges capacitor **712** up to $V_{dc} - V_{th}$, where $V_{th}$ is the threshold voltage of nMOSFET **702**. During this initial charging period, terminal **716** of nMOSFET **702** acts as a drain and terminal **708** acts as a source to nMOSFET **702**.

**[0026]** After charging capacitor **712** to $V_{dc} - V_{th}$, nMOSFET **702** will be in its sub-threshold region and will provide leakage current to capacitor **712**, with the gate-to-source voltage of nMOSFET **702** greater than zero. Denote the voltage at terminal **708** as $V_0$ (which is the same as the voltage on capacitor **712**). If $V_0 = V_{dc}$ and the excursions of the input signal voltage about $V_{dc}$ have peak values less than $V_{th}$ (e.g., $V_{ac} < V_{th}$), then it is seen that the charge provided to capacitor **712** during positive excursions of the input signal voltage about $V_{dc}$ and the charge removed from capacitor **712** during negative excursions of the input signal voltage about $V_{dc}$ each occur while nMOSFET **702** and nMOSFET **704** are in their sub-threshold regions. During charging, nMOSFET **702** has sub-threshold currents with its gate-to-source voltage greater than zero, and at the same time nMOSFET **704** charges with sub-threshold currents with its gate-to-source voltage at zero. During discharging, these roles are reversed, and nMOSFET **702** discharges with sub-threshold currents with its gate-to-source voltage at zero, and nMOSFET **704**

discharges node **708** with sub-threshold currents with its gate-to-source voltage greater than zero. Because of this symmetry, it is seen that the steady state voltage of capacitor **712** is the DC offset voltage $V_{dc}$. The steady state voltage will tend to track $V_{dc}$ if it varies. Thus, the circuit of Fig. 7 provides a local time-average of the input signal.

**[0027]** In contrast with the circuits of Figs 5. and 6, the circuit of Fig. 7 may provide a more accurate measure of the time-average (DC offset voltage) of the input signal. This accuracy may be limited by the sub-threshold current mismatch between nMOSFETs **702** and **704**. This matching may be superior, in some cases, to the matching of passive devices in deep sub-micron CMOS process technology

**[0028]** As an example, for one particular 0.13 micron process technology, it is found that the steady state capacitor voltage tracks $V_{dc}$ when the positive and negative excursions of the input signal voltage about $V_{dc}$ are within 50mV of $V_{th}$. For this particular process, $V_{th}$ may likely be in the range of 200mV, so that differential signals of up to 300mV peak-to-peak may be accommodated.

**[0029]** Thus, the circuits of Figs. 5, 6, and 7 provide a set of structures that may be used for evaluating the waveform parameters of local time-average maximum, local time-average minimum, and local time-average DC offset across a wide range of input signal levels. For some future process technologies, leakage current may be in excess of 1 micro ampere per micron of device width. This leakage current allows input voltages to be tracked at sub millisecond rates. The tracking rate may be controlled to be as slow as desired by adjusting the active devices length at minimum width, thus mitigating the need for a large capacitor. It should be appreciated that these numerical values are representative of one particular process technology, and may vary depending upon the particular process technology used for an embodiment.

**[0030]** Various modifications may be made to the disclosed embodiments without departing from the scope of the invention as claimed below.